```
sample-O0-arm:     file format elf32-littlearm


Disassembly of section .text:

00008000 <func2>:
    8000:       e1a0c00d        mov     ip, sp
    8004:       e92dd800        push    {fp, ip, lr, pc}
    8008:       e24cb004        sub     fp, ip, #4
    800c:       e24dd008        sub     sp, sp, #8
    8010:       e50b0010        str     r0, [fp, #-16]
    8014:       e50b1014        str     r1, [fp, #-20]
    8018:       e51b2010        ldr     r2, [fp, #-16]
    801c:       e51b3014        ldr     r3, [fp, #-20]
    8020:       e0823003        add     r3, r2, r3
    8024:       e1a00003        mov     r0, r3
    8028:       e24bd00c        sub     sp, fp, #12
    802c:       e89da800        ldm     sp, {fp, sp, pc}

00008030 <func>:
    8030:       e1a0c00d        mov     ip, sp
    8034:       e92dd800        push    {fp, ip, lr, pc}
    8038:       e24cb004        sub     fp, ip, #4
    803c:       e24dd008        sub     sp, sp, #8
    8040:       e50b0010        str     r0, [fp, #-16]
    8044:       e3e03811        mvn     r3, #1114112    ; 0x110000
    8048:       e2433c22        sub     r3, r3, #8704   ; 0x2200
    804c:       e2433033        sub     r3, r3, #51     ; 0x33
    8050:       e50b3014        str     r3, [fp, #-20]
    8054:       e59f2024        ldr     r2, [pc, #36]   ; 8080 <func+0x50>
    8058:       e51b3010        ldr     r3, [fp, #-16]
    805c:       e5823000        str     r3, [r2]
    8060:       e59f3018        ldr     r3, [pc, #24]   ; 8080 <func+0x50>
    8064:       e5930000        ldr     r0, [r3]
    8068:       e51b1014        ldr     r1, [fp, #-20]
    806c:       ebffffe3        bl      8000 <func2>
    8070:       e1a03000        mov     r3, r0
    8074:       e1a00003        mov     r0, r3
    8078:       e24bd00c        sub     sp, fp, #12
    807c:       e89da800        ldm     sp, {fp, sp, pc}
    8080:       000100bc        .word   0x000100bc

00008084 <main>:
    8084:       e1a0c00d        mov     ip, sp
    8088:       e92dd800        push    {fp, ip, lr, pc}
    808c:       e24cb004        sub     fp, ip, #4
    8090:       e24dd004        sub     sp, sp, #4
    8094:       e59f301c        ldr     r3, [pc, #28]   ; 80b8 <main+0x34>
    8098:       e50b3010        str     r3, [fp, #-16]
    809c:       e51b3010        ldr     r3, [fp, #-16]
    80a0:       e3a00014        mov     r0, #20
    80a4:       e1a0e00f        mov     lr, pc
    80a8:       e1a0f003        mov     pc, r3
    80ac:       e1a03000        mov     r3, r0
    80b0:       e1a00003        mov     r0, r3
    80b4:       e89da808        ldm     sp, {r3, fp, sp, pc}
    80b8:       00008030        .word   0x00008030
```

```
sample-O0-h8:     file format elf32-h8300


Disassembly of section .text:

00000100 <_func2>:
 100:   6d f6           mov.w   r6,@-r7
 102:   0d 76           mov.w   r7,r6
 104:   1b 87           subs    #2,r7
 106:   1b 87           subs    #2,r7
 108:   6f e0 ff fe     mov.w   r0,@(0xfffe:16,r6)
 10c:   6f e1 ff fc     mov.w   r1,@(0xfffc:16,r6)
 110:   6f 63 ff fe     mov.w   @(0xfffe:16,r6),r3
 114:   6f 62 ff fc     mov.w   @(0xfffc:16,r6),r2
 118:   09 32           add.w   r3,r2
 11a:   0d 20           mov.w   r2,r0
 11c:   0b 87           adds    #2,r7
 11e:   0b 87           adds    #2,r7
 120:   6d 76           mov.w   @r7+,r6
 122:   54 70           rts

00000124 <_func>:
 124:   6d f6           mov.w   r6,@-r7
 126:   0d 76           mov.w   r7,r6
 128:   1b 87           subs    #2,r7
 12a:   1b 87           subs    #2,r7
 12c:   6f e0 ff fe     mov.w   r0,@(0xfffe:16,r6)
 130:   79 02 dd cc     mov.w   #0xddcc,r2
 134:   6f e2 ff fc     mov.w   r2,@(0xfffc:16,r6)
 138:   6f 62 ff fe     mov.w   @(0xfffe:16,r6),r2
 13c:   6b 82 01 7a     mov.w   r2,@0x17a:16
 140:   6f 61 ff fc     mov.w   @(0xfffc:16,r6),r1
 144:   6b 00 01 7a     mov.w   @0x17a:16,r0
 148:   5e 00 01 00     jsr     @0x100:24
 14c:   0d 02           mov.w   r0,r2
 14e:   0d 20           mov.w   r2,r0
 150:   0b 87           adds    #2,r7
 152:   0b 87           adds    #2,r7
 154:   6d 76           mov.w   @r7+,r6
 156:   54 70           rts

00000158 <_main>:
 158:   6d f6           mov.w   r6,@-r7
 15a:   0d 76           mov.w   r7,r6
 15c:   1b 87           subs    #2,r7
 15e:   79 02 01 24     mov.w   #0x124,r2
 162:   6f e2 ff fe     mov.w   r2,@(0xfffe:16,r6)
 166:   6f 62 ff fe     mov.w   @(0xfffe:16,r6),r2
 16a:   79 00 00 14     mov.w   #0x14,r0
 16e:   5d 20           jsr     @r2
 170:   0d 02           mov.w   r0,r2
 172:   0d 20           mov.w   r2,r0
 174:   0b 87           adds    #2,r7
 176:   6d 76           mov.w   @r7+,r6
 178:   54 70           rts
```

```
sample-O0-i386:     file format elf32-i386-freebsd

Disassembly of section .text:

08048080 <func2>:
 8048080:       55                      push   %ebp
 8048081:       89 e5                   mov    %esp,%ebp
 8048083:       8b 45 0c                mov    0xc(%ebp),%eax
 8048086:       03 45 08                add    0x8(%ebp),%eax
 8048089:       5d                      pop    %ebp
 804808a:       c3                      ret
 804808b:       90                      nop
 804808c:       8d 74 26 00             lea    0x0(%esi),%esi

08048090 <func>:
 8048090:       55                      push   %ebp
 8048091:       89 e5                   mov    %esp,%ebp
 8048093:       83 ec 18                sub    $0x18,%esp
 8048096:       c7 45 fc cc dd ee ff    movl   $0xffeeddcc,0xfffffffc(%ebp)
 804809d:       8b 45 08                mov    0x8(%ebp),%eax
 80480a0:       a3 f0 90 04 08          mov    %eax,0x80490f0
 80480a5:       8b 15 f0 90 04 08       mov    0x80490f0,%edx
 80480ab:       8b 45 fc                mov    0xfffffffc(%ebp),%eax
 80480ae:       89 44 24 04             mov    %eax,0x4(%esp)
 80480b2:       89 14 24                mov    %edx,(%esp)
 80480b5:       e8 c6 ff ff ff          call   8048080 <func2>
 80480ba:       c9                      leave
 80480bb:       c3                      ret
 80480bc:       8d 74 26 00             lea    0x0(%esi),%esi

080480c0 <main>:
 80480c0:       8d 4c 24 04             lea    0x4(%esp),%ecx
 80480c4:       83 e4 f0                and    $0xfffffff0,%esp
 80480c7:       ff 71 fc                pushl  0xfffffffc(%ecx)
 80480ca:       55                      push   %ebp
 80480cb:       89 e5                   mov    %esp,%ebp
 80480cd:       51                      push   %ecx
 80480ce:       83 ec 14                sub    $0x14,%esp
 80480d1:       c7 45 f8 90 80 04 08    movl   $0x8048090,0xfffffff8(%ebp)
 80480d8:       c7 04 24 14 00 00 00    movl   $0x14,(%esp)
 80480df:       8b 45 f8                mov    0xfffffff8(%ebp),%eax
 80480e2:       ff d0                   call   *%eax
 80480e4:       83 c4 14                add    $0x14,%esp
 80480e7:       59                      pop    %ecx
 80480e8:       5d                      pop    %ebp
 80480e9:       8d 61 fc                lea    0xfffffffc(%ecx),%esp
 80480ec:       c3                      ret
```

```
sample-O0-mips:     file format elf32-bigmips


Disassembly of section .text:

00400000 <func2>:
  400000:       27bdfff8        addiu   sp,sp,-8
  400004:       afbe0000        sw      s8,0(sp)
  400008:       03a0f021        move    s8,sp
  40000c:       afc40008        sw      a0,8(s8)
  400010:       afc5000c        sw      a1,12(s8)
  400014:       8fc30008        lw      v1,8(s8)
  400018:       8fc2000c        lw      v0,12(s8)
  40001c:       00000000        nop
  400020:       00621021        addu    v0,v1,v0
  400024:       03c0e821        move    sp,s8
  400028:       8fbe0000        lw      s8,0(sp)
  40002c:       03e00008        jr      ra
  400030:       27bd0008        addiu   sp,sp,8

00400034 <func>:
  400034:       27bdffe0        addiu   sp,sp,-32
  400038:       afbf001c        sw      ra,28(sp)
  40003c:       afbe0018        sw      s8,24(sp)
  400040:       03a0f021        move    s8,sp
  400044:       afc40020        sw      a0,32(s8)
  400048:       3c02ffee        lui     v0,0xffee
  40004c:       3442ddcc        ori     v0,v0,0xddcc
  400050:       afc20010        sw      v0,16(s8)
  400054:       8fc20020        lw      v0,32(s8)
  400058:       00000000        nop
  40005c:       af828004        sw      v0,-32764(gp)
  400060:       8f848004        lw      a0,-32764(gp)
  400064:       8fc50010        lw      a1,16(s8)
  400068:       0c100000        jal     400000 <func2>
  40006c:       00000000        nop
  400070:       03c0e821        move    sp,s8
  400074:       8fbf001c        lw      ra,28(sp)
  400078:       8fbe0018        lw      s8,24(sp)
  40007c:       03e00008        jr      ra
  400080:       27bd0020        addiu   sp,sp,32

00400084 <main>:
  400084:       27bdffe0        addiu   sp,sp,-32
  400088:       afbf001c        sw      ra,28(sp)
  40008c:       afbe0018        sw      s8,24(sp)
  400090:       03a0f021        move    s8,sp
  400094:       3c020040        lui     v0,0x40
  400098:       24420034        addiu   v0,v0,52
  40009c:       afc20010        sw      v0,16(s8)
  4000a0:       8fc20010        lw      v0,16(s8)
  4000a4:       24040014        li      a0,20
  4000a8:       0040f809        jalr    v0
  4000ac:       00000000        nop
  4000b0:       03c0e821        move    sp,s8
  4000b4:       8fbf001c        lw      ra,28(sp)
  4000b8:       8fbe0018        lw      s8,24(sp)
  4000bc:       03e00008        jr      ra
  4000c0:       27bd0020        addiu   sp,sp,32
```

```
sample-O0-ppc:     file format elf32-powerpc


Disassembly of section .text:

01800074 <func2>:
 1800074:       94 21 ff e0     stwu    r1,-32(r1)
 1800078:       93 e1 00 1c     stw     r31,28(r1)
 180007c:       7c 3f 0b 78     mr      r31,r1
 1800080:       90 7f 00 08     stw     r3,8(r31)
 1800084:       90 9f 00 0c     stw     r4,12(r31)
 1800088:       81 3f 00 08     lwz     r9,8(r31)
 180008c:       80 1f 00 0c     lwz     r0,12(r31)
 1800090:       7c 09 02 14     add     r0,r9,r0
 1800094:       7c 03 03 78     mr      r3,r0
 1800098:       81 61 00 00     lwz     r11,0(r1)
 180009c:       83 eb ff fc     lwz     r31,-4(r11)
 18000a0:       7d 61 5b 78     mr      r1,r11
 18000a4:       4e 80 00 20     blr

018000a8 <func>:
 18000a8:       94 21 ff e0     stwu    r1,-32(r1)
 18000ac:       7c 08 02 a6     mflr    r0
 18000b0:       93 e1 00 1c     stw     r31,28(r1)
 18000b4:       90 01 00 24     stw     r0,36(r1)
 18000b8:       7c 3f 0b 78     mr      r31,r1
 18000bc:       90 7f 00 08     stw     r3,8(r31)
 18000c0:       3c 00 ff ee     lis     r0,-18
 18000c4:       60 00 dd cc     ori     r0,r0,56780
 18000c8:       90 1f 00 0c     stw     r0,12(r31)
 18000cc:       3d 20 01 81     lis     r9,385
 18000d0:       80 1f 00 08     lwz     r0,8(r31)
 18000d4:       90 09 01 58     stw     r0,344(r9)
 18000d8:       3d 20 01 81     lis     r9,385
 18000dc:       80 69 01 58     lwz     r3,344(r9)
 18000e0:       80 9f 00 0c     lwz     r4,12(r31)
 18000e4:       4b ff ff 91     bl      1800074 <func2>
 18000e8:       7c 60 1b 78     mr      r0,r3
 18000ec:       7c 03 03 78     mr      r3,r0
 18000f0:       81 61 00 00     lwz     r11,0(r1)
 18000f4:       80 0b 00 04     lwz     r0,4(r11)
 18000f8:       7c 08 03 a6     mtlr    r0
 18000fc:       83 eb ff fc     lwz     r31,-4(r11)
 1800100:       7d 61 5b 78     mr      r1,r11
 1800104:       4e 80 00 20     blr

01800108 <main>:
 1800108:       94 21 ff e0     stwu    r1,-32(r1)
 180010c:       7c 08 02 a6     mflr    r0
 1800110:       93 e1 00 1c     stw     r31,28(r1)
 1800114:       90 01 00 24     stw     r0,36(r1)
 1800118:       7c 3f 0b 78     mr      r31,r1
 180011c:       3d 20 01 80     lis     r9,384
 1800120:       38 09 00 a8     addi    r0,r9,168
 1800124:       90 1f 00 08     stw     r0,8(r31)
 1800128:       80 1f 00 08     lwz     r0,8(r31)
 180012c:       7c 09 03 a6     mtctr   r0
 1800130:       38 60 00 14     li      r3,20
 1800134:       4e 80 04 21     bctrl
 1800138:       7c 60 1b 78     mr      r0,r3
 180013c:       7c 03 03 78     mr      r3,r0
 1800140:       81 61 00 00     lwz     r11,0(r1)
 1800144:       80 0b 00 04     lwz     r0,4(r11)
 1800148:       7c 08 03 a6     mtlr    r0
 180014c:       83 eb ff fc     lwz     r31,-4(r11)
```



```
 1800150:       7d 61 5b 78     mr      r1,r11
 1800154:       4e 80 00 20     blr
```

```
sample-O0-sh:     file format elf32-sh


Disassembly of section .text:

00001000 <_func2>:
    1000:       2f e6           mov.l   r14,@-r15
    1002:       4f 22           sts.l   pr,@-r15
    1004:       7f f8           add     #-8,r15
    1006:       6e f3           mov     r15,r14
    1008:       2e 42           mov.l   r4,@r14
    100a:       1e 51           mov.l   r5,@(4,r14)
    100c:       62 e2           mov.l   @r14,r2
    100e:       51 e1           mov.l   @(4,r14),r1
    1010:       31 2c           add     r2,r1
    1012:       60 13           mov     r1,r0
    1014:       7e 08           add     #8,r14
    1016:       6f e3           mov     r14,r15
    1018:       4f 26           lds.l   @r15+,pr
    101a:       6e f6           mov.l   @r15+,r14
    101c:       00 0b           rts
    101e:       00 09           nop

00001020 <_func>:
    1020:       2f e6           mov.l   r14,@-r15
    1022:       4f 22           sts.l   pr,@-r15
    1024:       7f f8           add     #-8,r15
    1026:       6e f3           mov     r15,r14
    1028:       2e 42           mov.l   r4,@r14
    102a:       d1 09           mov.l   1050 <_func+0x30>,r1    ! ffeeddcc
    102c:       1e 11           mov.l   r1,@(4,r14)
    102e:       d2 09           mov.l   1054 <_func+0x34>,r2    ! 1080 <___ctors>
    1030:       61 e2           mov.l   @r14,r1
    1032:       22 12           mov.l   r1,@r2
    1034:       d1 07           mov.l   1054 <_func+0x34>,r1    ! 1080 <___ctors>
    1036:       52 e1           mov.l   @(4,r14),r2
    1038:       64 12           mov.l   @r1,r4
    103a:       65 23           mov     r2,r5
    103c:       d1 06           mov.l   1058 <_func+0x38>,r1    ! 1000 <_func2>
    103e:       41 0b           jsr     @r1
    1040:       00 09           nop
    1042:       7e 08           add     #8,r14
    1044:       6f e3           mov     r14,r15
    1046:       4f 26           lds.l   @r15+,pr
    1048:       6e f6           mov.l   @r15+,r14
    104a:       00 0b           rts
    104c:       00 09           nop
    104e:       00 09           nop
    1050:       ff ee           .word 0xffee
    1052:       dd cc           mov.l   1384 <_end+0x300>,r13
    1054:       00 00           .word 0x0000
    1056:       10 80           mov.l   r8,@(0,r0)
    1058:       00 00           .word 0x0000
    105a:       10 00           mov.l   r0,@(0,r0)

0000105c <_main>:
    105c:       2f e6           mov.l   r14,@-r15
    105e:       4f 22           sts.l   pr,@-r15
    1060:       7f fc           add     #-4,r15
    1062:       6e f3           mov     r15,r14
    1064:       d1 05           mov.l   107c <_main+0x20>,r1    ! 1020 <_func>
    1066:       2e 12           mov.l   r1,@r14
    1068:       61 e2           mov.l   @r14,r1
    106a:       e4 14           mov     #20,r4
    106c:       41 0b           jsr     @r1
```



```
    106e:       00 09           nop
    1070:       7e 04           add     #4,r14
    1072:       6f e3           mov     r14,r15
    1074:       4f 26           lds.l   @r15+,pr
    1076:       6e f6           mov.l   @r15+,r14
    1078:       00 0b           rts
    107a:       00 09           nop
    107c:       00 00           .word 0x0000
    107e:       10 20           mov.l   r2,@(0,r0)
```

```
sample-O1-arm:     file format elf32-littlearm


Disassembly of section .text:

00008000 <func2>:
    8000:       e0800001        add     r0, r0, r1
    8004:       e1a0f00e        mov     pc, lr

00008008 <func>:
    8008:       e1a0c00d        mov     ip, sp
    800c:       e92dd800        push    {fp, ip, lr, pc}
    8010:       e24cb004        sub     fp, ip, #4
    8014:       e59f3014        ldr     r3, [pc, #20]   ; 8030 <func+0x28>
    8018:       e5830000        str     r0, [r3]
    801c:       e3e01811        mvn     r1, #1114112    ; 0x110000
    8020:       e2411c22        sub     r1, r1, #8704   ; 0x2200
    8024:       e2411033        sub     r1, r1, #51     ; 0x33
    8028:       ebfffff4        bl      8000 <func2>
    802c:       e89da800        ldm     sp, {fp, sp, pc}
    8030:       0001004c        .word   0x0001004c

00008034 <main>:
    8034:       e1a0c00d        mov     ip, sp
    8038:       e92dd800        push    {fp, ip, lr, pc}
    803c:       e24cb004        sub     fp, ip, #4
    8040:       e3a00014        mov     r0, #20
    8044:       ebffffef        bl      8008 <func>
    8048:       e89da800        ldm     sp, {fp, sp, pc}
```

```
sample-O1-h8:     file format elf32-h8300


Disassembly of section .text:

00000100 <_func2>:
 100:   6d f6           mov.w   r6,@-r7
 102:   0d 76           mov.w   r7,r6
 104:   09 10           add.w   r1,r0
 106:   6d 76           mov.w   @r7+,r6
 108:   54 70           rts

0000010a <_func>:
 10a:   6d f6           mov.w   r6,@-r7
 10c:   0d 76           mov.w   r7,r6
 10e:   6b 80 01 2e     mov.w   r0,@0x12e:16
 112:   79 01 dd cc     mov.w   #0xddcc,r1
 116:   5e 00 01 00     jsr     @0x100:24
 11a:   6d 76           mov.w   @r7+,r6
 11c:   54 70           rts

0000011e <_main>:
 11e:   6d f6           mov.w   r6,@-r7
 120:   0d 76           mov.w   r7,r6
 122:   79 00 00 14     mov.w   #0x14,r0
 126:   5e 00 01 0a     jsr     @0x10a:24
 12a:   6d 76           mov.w   @r7+,r6
 12c:   54 70           rts
```

```
sample-O1-i386:     file format elf32-i386-freebsd

Disassembly of section .text:

08048080 <func2>:
 8048080:       55                      push   %ebp
 8048081:       89 e5                   mov    %esp,%ebp
 8048083:       8b 45 0c                mov    0xc(%ebp),%eax
 8048086:       03 45 08                add    0x8(%ebp),%eax
 8048089:       5d                      pop    %ebp
 804808a:       c3                      ret
 804808b:       90                      nop
 804808c:       8d 74 26 00             lea    0x0(%esi),%esi

08048090 <func>:
 8048090:       55                      push   %ebp
 8048091:       89 e5                   mov    %esp,%ebp
 8048093:       83 ec 08                sub    $0x8,%esp
 8048096:       8b 45 08                mov    0x8(%ebp),%eax
 8048099:       a3 d8 90 04 08          mov    %eax,0x80490d8
 804809e:       c7 44 24 04 cc dd ee    movl   $0xffeeddcc,0x4(%esp)
 80480a5:       ff
 80480a6:       89 04 24                mov    %eax,(%esp)
 80480a9:       e8 d2 ff ff ff          call   8048080 <func2>
 80480ae:       c9                      leave
 80480af:       c3                      ret

080480b0 <main>:
 80480b0:       8d 4c 24 04             lea    0x4(%esp),%ecx
 80480b4:       83 e4 f0                and    $0xfffffff0,%esp
 80480b7:       ff 71 fc                pushl  0xfffffffc(%ecx)
 80480ba:       55                      push   %ebp
 80480bb:       89 e5                   mov    %esp,%ebp
 80480bd:       51                      push   %ecx
 80480be:       83 ec 04                sub    $0x4,%esp
 80480c1:       c7 04 24 14 00 00 00    movl   $0x14,(%esp)
 80480c8:       e8 c3 ff ff ff          call   8048090 <func>
 80480cd:       83 c4 04                add    $0x4,%esp
 80480d0:       59                      pop    %ecx
 80480d1:       5d                      pop    %ebp
 80480d2:       8d 61 fc                lea    0xfffffffc(%ecx),%esp
 80480d5:       c3                      ret
```

```
sample-O1-mips:     file format elf32-bigmips


Disassembly of section .text:

00400000 <func2>:
  400000:       03e00008        jr      ra
  400004:       00851021        addu    v0,a0,a1

00400008 <func>:
  400008:       27bdffe8        addiu   sp,sp,-24
  40000c:       afbf0010        sw      ra,16(sp)
  400010:       af848010        sw      a0,-32752(gp)
  400014:       3c05ffee        lui     a1,0xffee
  400018:       0c100000        jal     400000 <func2>
  40001c:       34a5ddcc        ori     a1,a1,0xddcc
  400020:       8fbf0010        lw      ra,16(sp)
  400024:       00000000        nop
  400028:       03e00008        jr      ra
  40002c:       27bd0018        addiu   sp,sp,24

00400030 <main>:
  400030:       27bdffe8        addiu   sp,sp,-24
  400034:       afbf0010        sw      ra,16(sp)
  400038:       0c100002        jal     400008 <func>
  40003c:       24040014        li      a0,20
  400040:       8fbf0010        lw      ra,16(sp)
  400044:       00000000        nop
  400048:       03e00008        jr      ra
  40004c:       27bd0018        addiu   sp,sp,24
```

```
sample-O1-ppc:     file format elf32-powerpc


Disassembly of section .text:

01800074 <func2>:
 1800074:       7c 63 22 14     add     r3,r3,r4
 1800078:       4e 80 00 20     blr

0180007c <func>:
 180007c:       94 21 ff f0     stwu    r1,-16(r1)
 1800080:       7c 08 02 a6     mflr    r0
 1800084:       90 01 00 14     stw     r0,20(r1)
 1800088:       3d 20 01 81     lis     r9,385
 180008c:       90 69 00 d0     stw     r3,208(r9)
 1800090:       3c 80 ff ee     lis     r4,-18
 1800094:       60 84 dd cc     ori     r4,r4,56780
 1800098:       4b ff ff dd     bl      1800074 <func2>
 180009c:       80 01 00 14     lwz     r0,20(r1)
 18000a0:       7c 08 03 a6     mtlr    r0
 18000a4:       38 21 00 10     addi    r1,r1,16
 18000a8:       4e 80 00 20     blr

018000ac <main>:
 18000ac:       94 21 ff f0     stwu    r1,-16(r1)
 18000b0:       7c 08 02 a6     mflr    r0
 18000b4:       90 01 00 14     stw     r0,20(r1)
 18000b8:       38 60 00 14     li      r3,20
 18000bc:       4b ff ff c1     bl      180007c <func>
 18000c0:       80 01 00 14     lwz     r0,20(r1)
 18000c4:       7c 08 03 a6     mtlr    r0
 18000c8:       38 21 00 10     addi    r1,r1,16
 18000cc:       4e 80 00 20     blr
```

```
sample-O1-sh:     file format elf32-sh


Disassembly of section .text:

00001000 <_func2>:
    1000:       2f e6           mov.l   r14,@-r15
    1002:       4f 22           sts.l   pr,@-r15
    1004:       6e f3           mov     r15,r14
    1006:       60 43           mov     r4,r0
    1008:       30 5c           add     r5,r0
    100a:       6f e3           mov     r14,r15
    100c:       4f 26           lds.l   @r15+,pr
    100e:       00 0b           rts
    1010:       6e f6           mov.l   @r15+,r14

00001012 <_func>:
    1012:       2f e6           mov.l   r14,@-r15
    1014:       4f 22           sts.l   pr,@-r15
    1016:       6e f3           mov     r15,r14
    1018:       d1 04           mov.l   102c <_func+0x1a>,r1    ! 10d0 <___ctors>
    101a:       d5 05           mov.l   1030 <_func+0x1e>,r5    ! ffeeddcc
    101c:       d0 05           mov.l   1034 <_func+0x22>,r0    ! 1000 <_func2>
    101e:       40 0b           jsr     @r0
    1020:       21 42           mov.l   r4,@r1
    1022:       6f e3           mov     r14,r15
    1024:       4f 26           lds.l   @r15+,pr
    1026:       00 0b           rts
    1028:       6e f6           mov.l   @r15+,r14
    102a:       00 09           nop
    102c:       00 00           .word 0x0000
    102e:       10 d0           mov.l   r13,@(0,r0)
    1030:       ff ee           .word 0xffee
    1032:       dd cc           mov.l   1364 <_end+0x290>,r13
    1034:       00 00           .word 0x0000
    1036:       10 00           mov.l   r0,@(0,r0)

00001038 <_main>:
    1038:       2f e6           mov.l   r14,@-r15
    103a:       4f 22           sts.l   pr,@-r15
    103c:       6e f3           mov     r15,r14
    103e:       d0 03           mov.l   104c <_main+0x14>,r0    ! 1012 <_func>
    1040:       40 0b           jsr     @r0
    1042:       e4 14           mov     #20,r4
    1044:       6f e3           mov     r14,r15
    1046:       4f 26           lds.l   @r15+,pr
    1048:       00 0b           rts
    104a:       6e f6           mov.l   @r15+,r14
    104c:       00 00           .word 0x0000
    104e:       10 12           mov.l   r1,@(8,r0)
```